

**Response**

Applicant: Dale C. Morris et al.

Serial No.: 09/499,720

Filed: February 8, 2000

Docket No.: 10991915-1 (H300.121.101)

Title: PRIVILEGE PROMOTION BASED ON CHECK OF PREVIOUS PRIVILEGE LEVEL

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**REMARKS**

The following remarks are made in response to the Office Action mailed February 1, 2005. Claims 1-24 were rejected. With this Response, no claims have been amended. Claims 1-24 remain pending in the application and are presented for reconsideration and allowance.

**Claim Rejections under 35 U.S.C. § 102**

The Examiner rejected claims 1-24 under 35 U.S.C. § 102(e) as being anticipated by Arora, U.S. Patent No. 6,393,556.

Applicants submit that the Arora Patent does not teach or suggest the invention of independent claims 1, 6, 12, 17, and 23.

The Arora Patent discloses changing a privilege level in a processor configured to pipeline instructions. The processor includes a first memory storing an architectural privilege level that is set at a first privilege level, a second memory storing a plurality of instructions, and a pipeline including a plurality of processing stages. A first instruction is fetched from the memory and a determination is made whether the first instruction requires the first privilege level be changed to a second privilege level, and in response thereto, any subsequent instructions are flushed from the pipeline before recording the second privilege level in the first memory. (Abstract).

The processor 30 maintains a "current privilege level" ("CPL") 38 in a memory storage device. The CPL is maintained in the processor's register set. The operating system sets the CPL to prevent the user from performing dangerous or insecure operations. If the pipeline 30 is currently processing an application program instruction, a prior instruction would have set the CPL 38 to the proper privilege level. If an instruction requiring a higher privilege level follows the current instruction, an instruction, such as an "enter privilege code" ("EPC") instruction, that directs the processor to change the privilege level of the CPL must first be processed to increase the privilege level. (Col. 4, lines 13-27).

After decoding an instruction directing the processor to change the CPL 38 from a first to a second privilege level, the processor compares the second privilege level to the CPL 38. (Col. 6, lines 27-31). The processor will compare the CPL 38 with the privilege level specified in the EPC instruction. If the EPC instruction directs the processor to change the

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CPL 38 to a higher privilege level, the processor flushes any instructions in the pipeline subsequent to the EPC instruction, and continues processing the EPC instruction. When the EPC instruction is retired, the CPL 38 privilege level is increased. If the EPC instruction specifies a privilege level lower than or the same as the CPL 38, the processor will issue a fault. (Col. 6, lines 46-59).

Applicants submit that the Arora Patent does not teach or suggest the method of independent claim 1. The Arora Patent fails to disclose **performing a privilege promotion instruction by the operating system, the privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level, the privilege promotion instruction including: reading a stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privilege than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level.**

The Examiner submits that the claim 1 limitation of the privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level is disclosed by the Arora Patent by "privilege level stored in the architectural register set." (Office Action, page 2). The architectural CPL 38 disclosed in the Arora Patent is what is stored in the architectural register set. This claim 1 limitation, however, is not referring to the storage of the privilege level, but rather to the storage of the privilege promotion instruction in a first page of memory not writeable by application instructions at a first privilege level. The Arora Patent does not teach or suggest storing a privileged promotion instruction in a first page of memory not writeable by application instructions at a first privilege level as recited in claim 1.

The Examiner submits that the claim 1 limitation of reading a stored previous privilege level state and comparing the read previous privilege level state to the current privilege level is disclosed in column 6, lines 46-49 of the Arora Patent. The cited text of the Arora Patent discloses comparing the architectural CPL with the privilege level specified in the EPC instruction. (Col. 6, lines 46-49). The Arora Patent fails to disclose the claim 1 limitation of reading a stored previous privilege level state and comparing the read previous privilege level state to the current privilege level. In the Arora Patent, a previous privilege

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level state is not stored and therefore cannot be read. The Arora Patent also discloses that the CPL is compared to the privilege level specified in the EPC instruction. In contrast, claim 1 requires comparing the read previous privilege level state to the current privilege level.

The Examiner submits that the claim 1 limitation of if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level is disclosed by the Arora Patent by "increase the architectural current privilege level from privilege level 3 to privilege level 0." (Office Action, page 3). The Arora Patent discloses raising the current architectural CPL to the privilege level specified in the EPC instruction. (Col. 6, lines 46-49). The Arora Patent, however, does not disclose the claim 1 limitation of promoting the current privilege level to a second privilege level which is higher than the first privilege level if the previous privilege level state is equal to or less privileged than the current privilege level.

In view of the above, Applicants believe independent claim 1 to be allowable over the Arora Patent. Dependent claims 2-5 further define patentably distinct independent claim 1. Accordingly, dependent claims 2-5 are also believed to be allowable over the art of record.

Applicants submit that the Arora Patent does not teach or suggest the method of independent claim 6. The Arora Patent fails to disclose **performing a call instruction to a second page of memory not writeable by the application instructions at the first privilege level, the call instruction including: storing a return address to the first page of memory; and storing the first privilege level in a previous privilege level state; and performing a privilege promotion instruction by the operating system, the privilege promotion instruction being stored in the second page of memory, the privilege promotion instruction including: reading the stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level.**

For the same reasons as discussed above with reference to independent claim 1, the Arora Patent fails to teach or suggest the limitations of claim 6 which are similar to the above

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limitations of claim 1. In addition, the Arora Patent fails to teach or suggest the limitations of claim 6 of storing a return address to the first page of memory.

In view of the above, Applicants believe independent claim 6 to be allowable over the cited reference. Dependent claims 7-11 further define patentably distinct independent claim 6. Accordingly, dependent claims 7-11 are also believed to be allowable over the art of record.

Applicants submit that the Arora Patent does not teach or suggest the computer system of claim 12 or 17 or the computer readable medium of claim 23. Regarding claim 12, the Arora Patent fails to disclose **a memory having a plurality of memory pages including a first memory page storing a privilege promotion instruction, wherein the first memory page is not writeable by application instructions at a first privilege level; and performing the privilege promotion instruction as follows: reads the previous level state; compares the read previously privilege state to the current privilege level; and if the previous privilege level state is equal to or less privilege than the current privilege level, promotes the current privilege level to a second privilege level which is higher than a first privilege level.**

Regarding claim 17, the Arora Patent fails to disclose **a memory having a plurality of memory pages including a first memory page storing application instructions and a second memory page storing a higher privilege routine and a privilege promotion instruction, wherein the second memory page is not writeable by the application instructions at a first privilege level; wherein the processor executes the application instructions with the current privilege level equal to the first privilege level and the application instructions perform a call instruction to the second memory page as follows: stores the return address to the first memory page; and stores the first privilege level in a previous privilege level state; and wherein the operating system performs the privilege promotion instruction as follows: reads the stored previous privilege level state; compares the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privilege than the current privilege level, promotes the current privilege level to a second privilege level which is higher than the first privilege level.**

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Regarding claim 23, the Arora Patent fails to disclose **reading a stored previous privilege state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a privilege level which is higher than the current privilege level.**

For the same reasons as discussed above with reference to independent claim 1, the Arora Patent fails to teach or suggest the limitations of independent claims 12, 17, and 23 which are similar to the above limitations of claim 1. In addition, independent claim 17, similar to independent claim 6, specifically includes the limitations of storing a return address to the first memory page which is not taught or suggested by the Arora Patent.

In view of the above, Applicants believe independent claims 12, 17, and 23 to be allowable over the cited reference. Dependent claims 13-16 further define patentably distinct independent claim 12. Dependent claims 18-22 further define patentably distinct independent claim 17. Dependent claim 24 further defines patentably distinct independent claim 23. Accordingly, dependent claims 13-16, 18-22, and 24 are also believed to be allowable over the art of record.

In view of the above, Applicants respectfully request that the rejections to claims 1-24 under 35 U.S.C. § 102(e) be withdrawn and that claims 1-24 be allowed.

**CONCLUSION**

In view of the above, Applicants respectfully submit that pending claims 1-24 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-24 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 08-2025.

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The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Response should be directed to either David A. Plettner at Telephone No. (408) 447-3013, Facsimile No. (408) 447-0854 or Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

**Hewlett-Packard Company**  
Intellectual Property Administration  
P.O. Box 272400  
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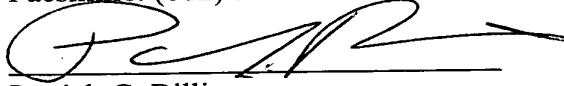
Respectfully submitted,

Dale C. Morris et al.

By their attorneys,

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**CERTIFICATE UNDER 37 C.F.R. 1.8:** The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 2 day of May, 2005.

By   
Name: Patrick G. Billig